FIG. 1

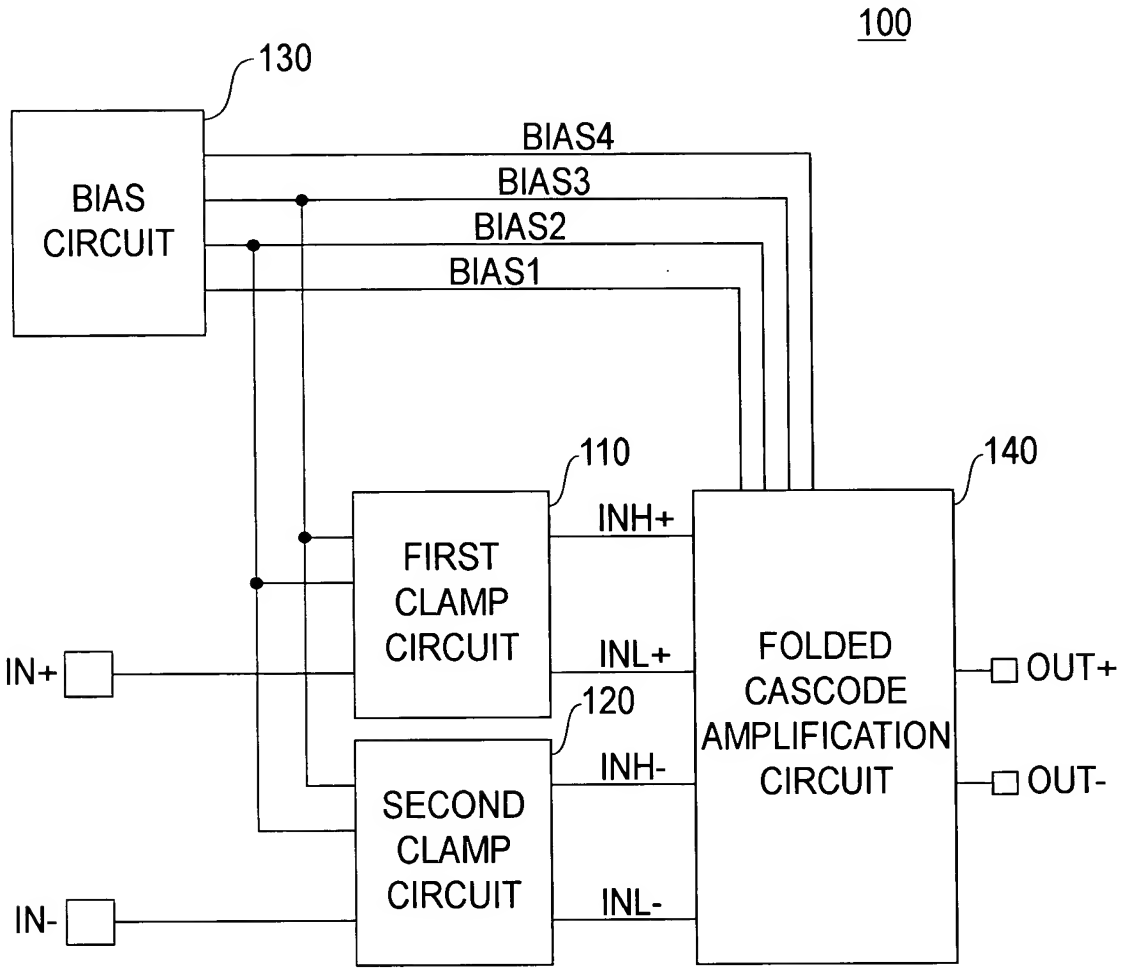
100
130
BIAS CIRCUIT
BIAS4
BIAS3
BIAS2
BIAS1
110
140
FIRST CLAMP CIRCUIT
INH+
INL+
FOLDED CASCODE AMPLIFICATION CIRCUIT
IN+
OUT+
120
INH-
SECOND CLAMP CIRCUIT
OUT-
IN-
INL-

FIG.2A

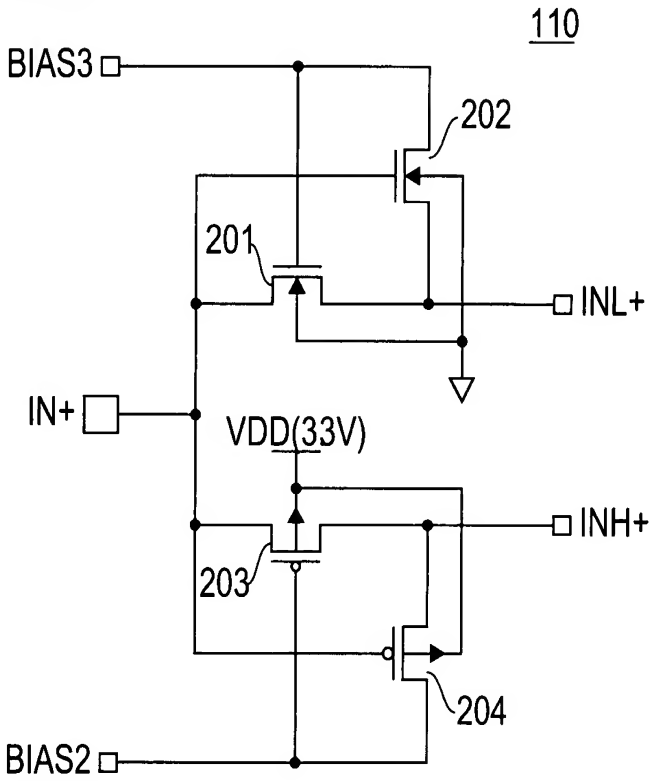
110
BIAS3
202
201
INL+
IN+
VDD(33V)
INH+
203
204
BIAS2

FIG.2B

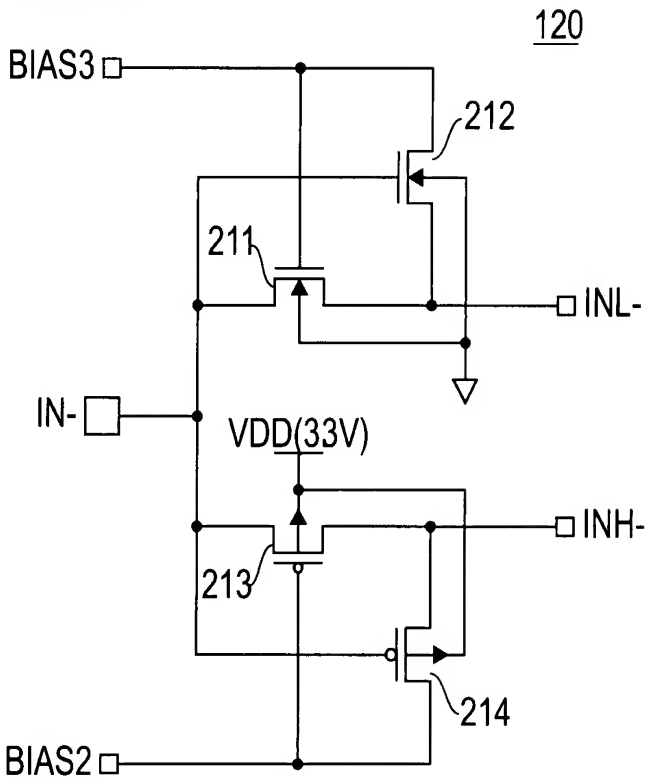
120
BIAS3
212
211
INL-
IN-
VDD(33V)
INH-
213
214
BIAS2

FIG.3

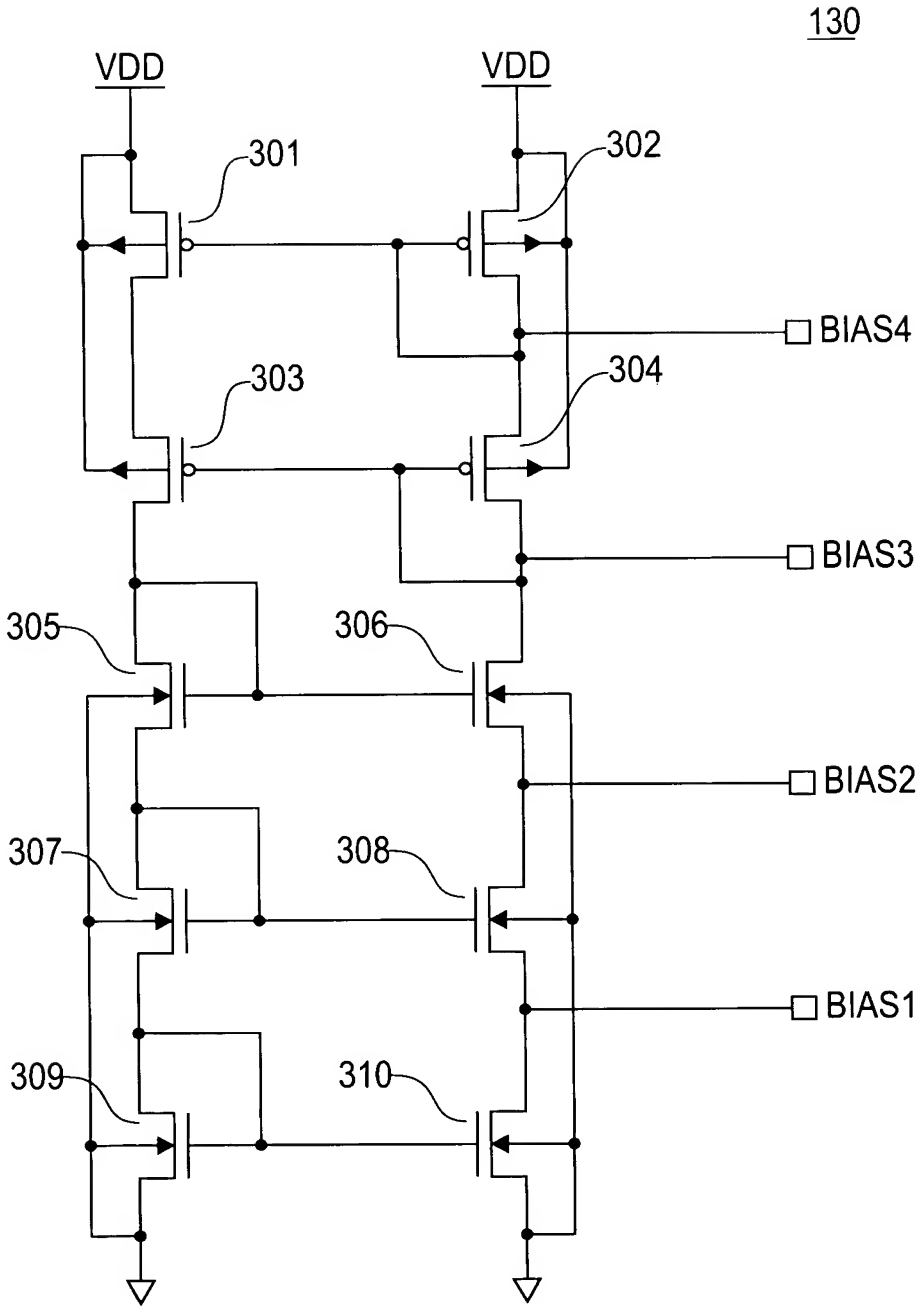
130
VDD
VDD
301
302
BIAS4
303
304
BIAS3
305
306
BIAS2
307
308
BIAS1
309
310

FIG. 4

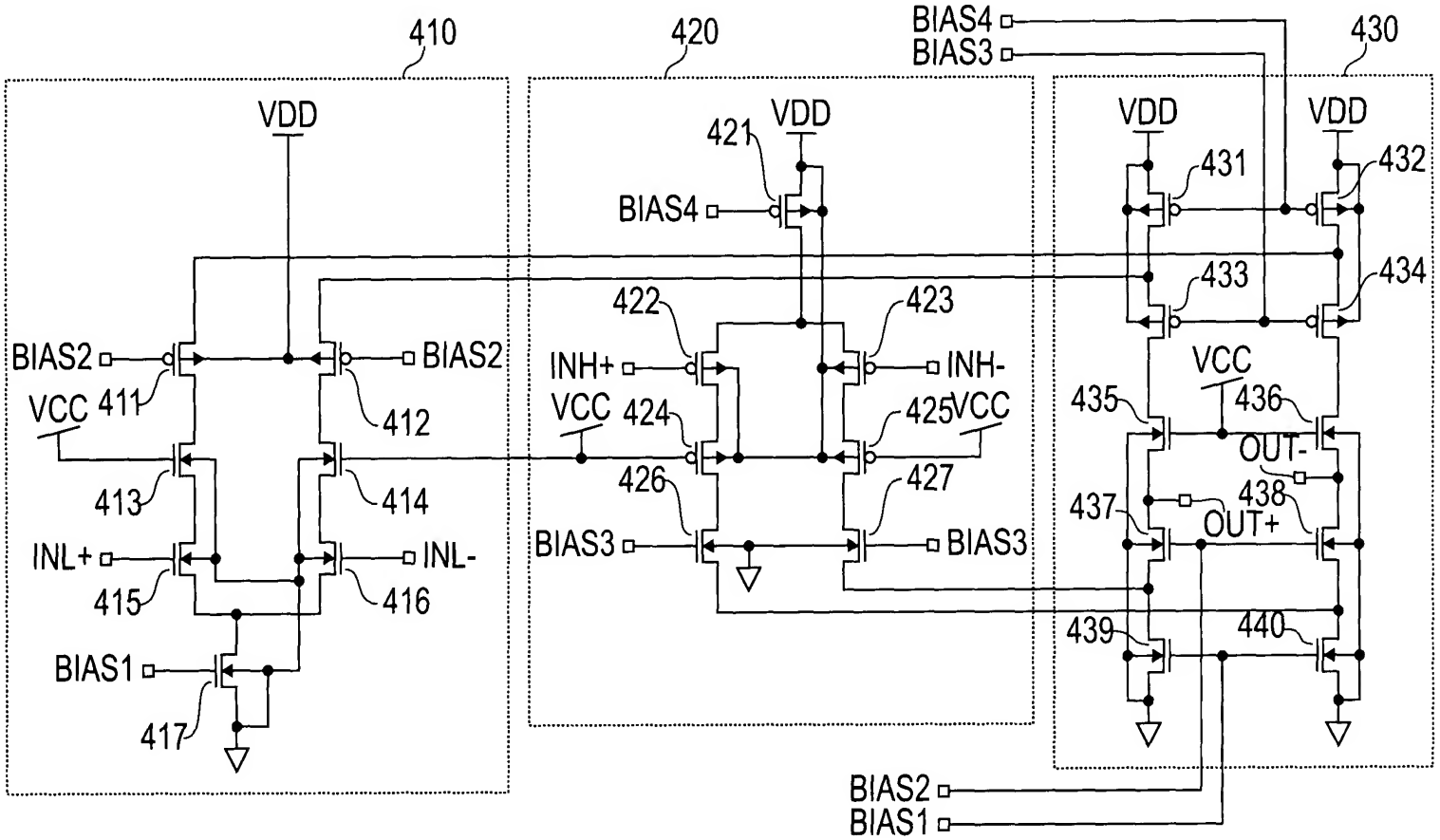
140
410
420
430
BIAS4
BIAS3
VDD
VDD
VDD
VDD
421
431
432
BIAS4
433
434
422
423
BIAS2
BIAS2
INH+
INH-
VCC 411
VCC 424
425 VCC
VCC
435
436
412
OUT-
413
414
426
427
438
437
OUT+
INL+
INL-
BIAS3
BIAS3
415
416
439
440
BIAS1
417
BIAS2
BIAS1

FIG.5

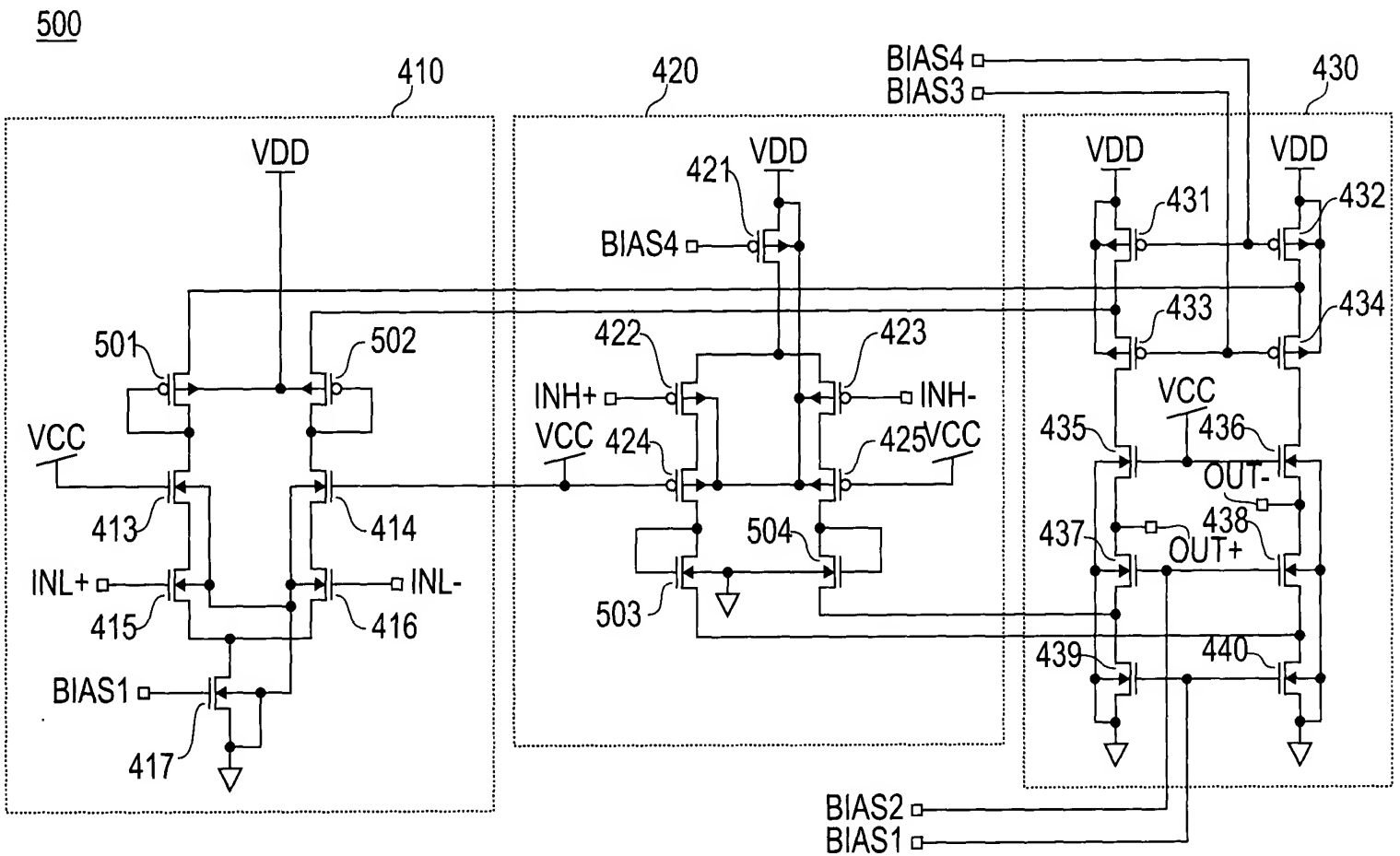
500
410
420
430
BIAS4
BIAS3
VDD
421
BIAS4
501
502
422
423
INH+
INH-
VCC
424
425
413
414
504
INL+
INL-
415
416
503
BIAS1
417
431
432
433
434
435
436
OUT-
437
438
OUT+
439
440
BIAS2
BIAS1

FIG.6

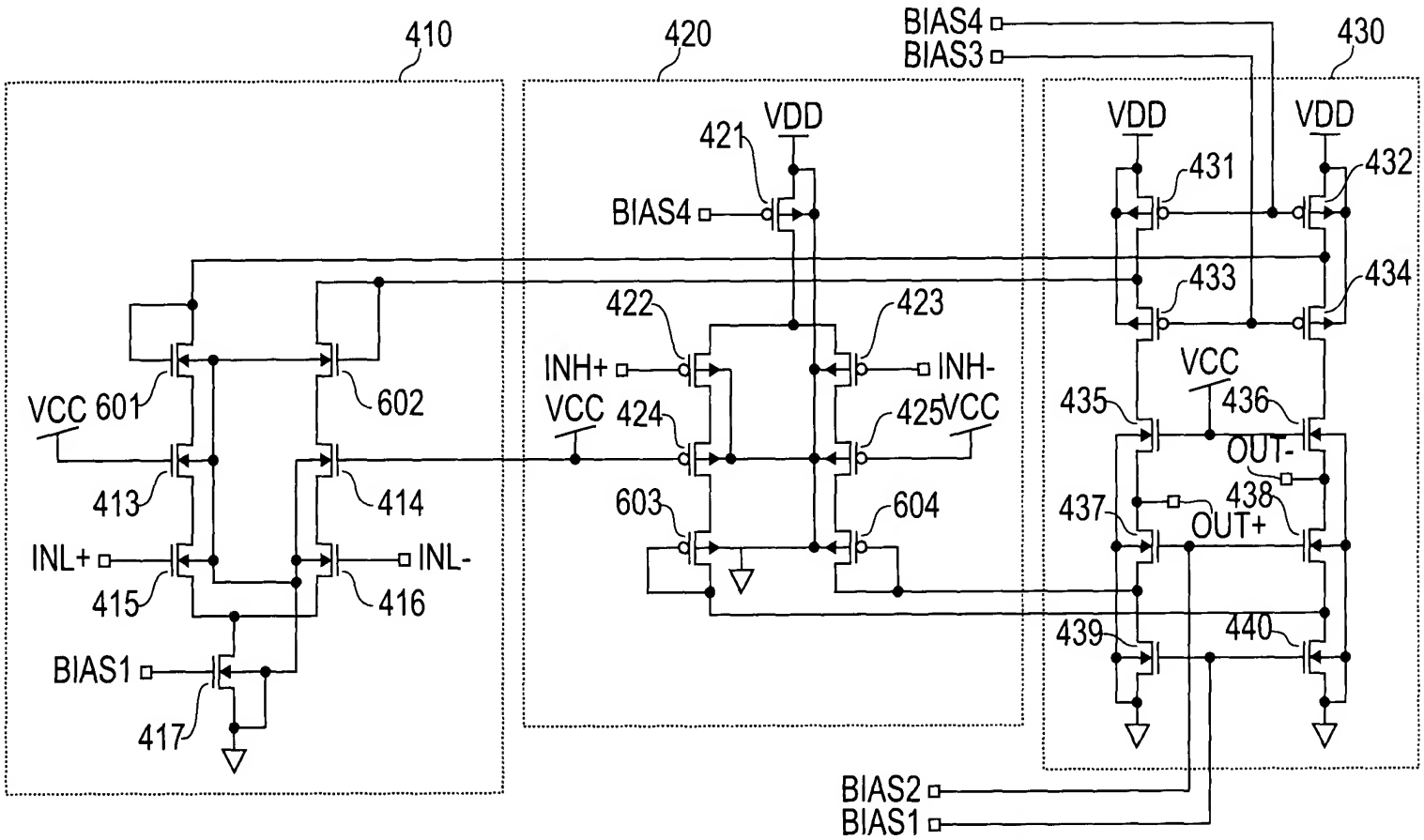
600
410
420
430
BIAS4
BIAS3
VDD
421
BIAS4
VDD
VDD
431
432
433
434
422
423
INH+
INH-
VCC 601
602
VCC
424
425
VCC
VCC
435
436
OUT-
413
414
603
604
437
438
OUT+
INL+
INL-
415
416
439
440
BIAS1
417
BIAS2
BIAS1

FIG. 7

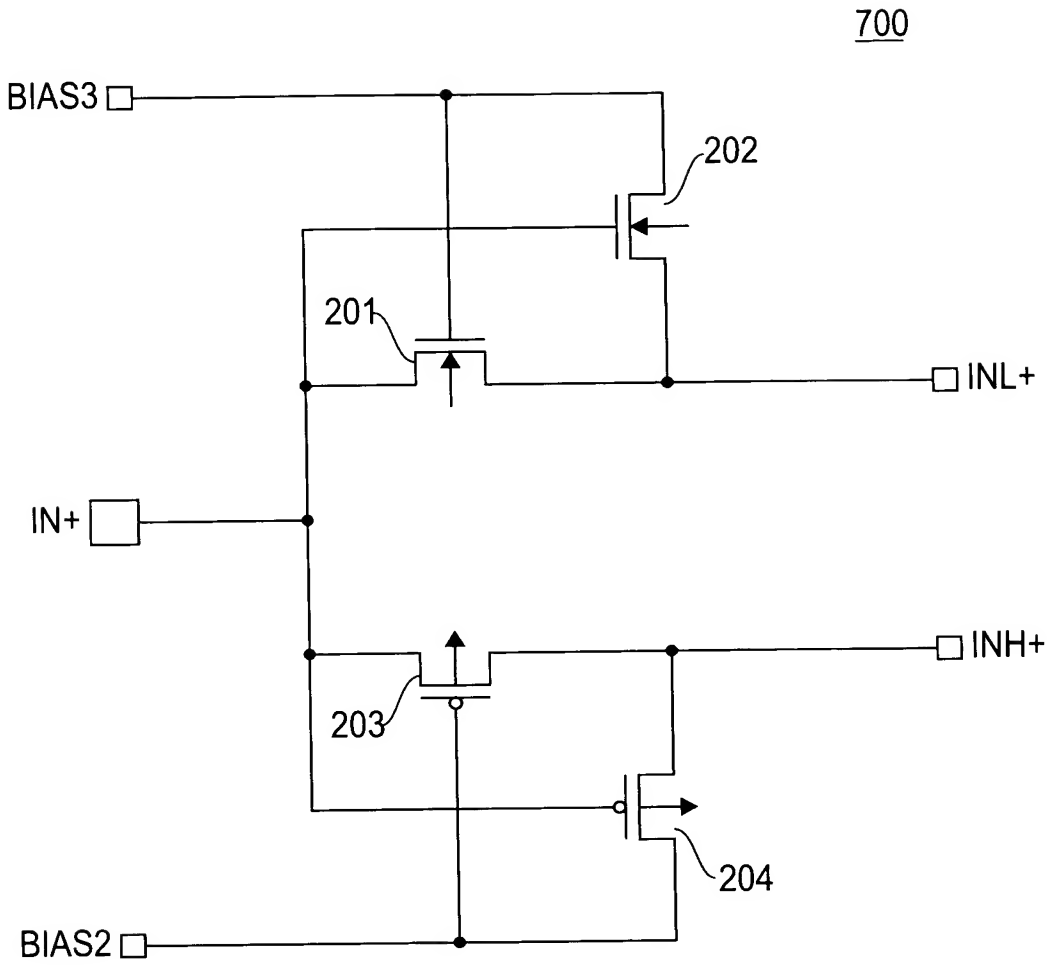

FIG. 8

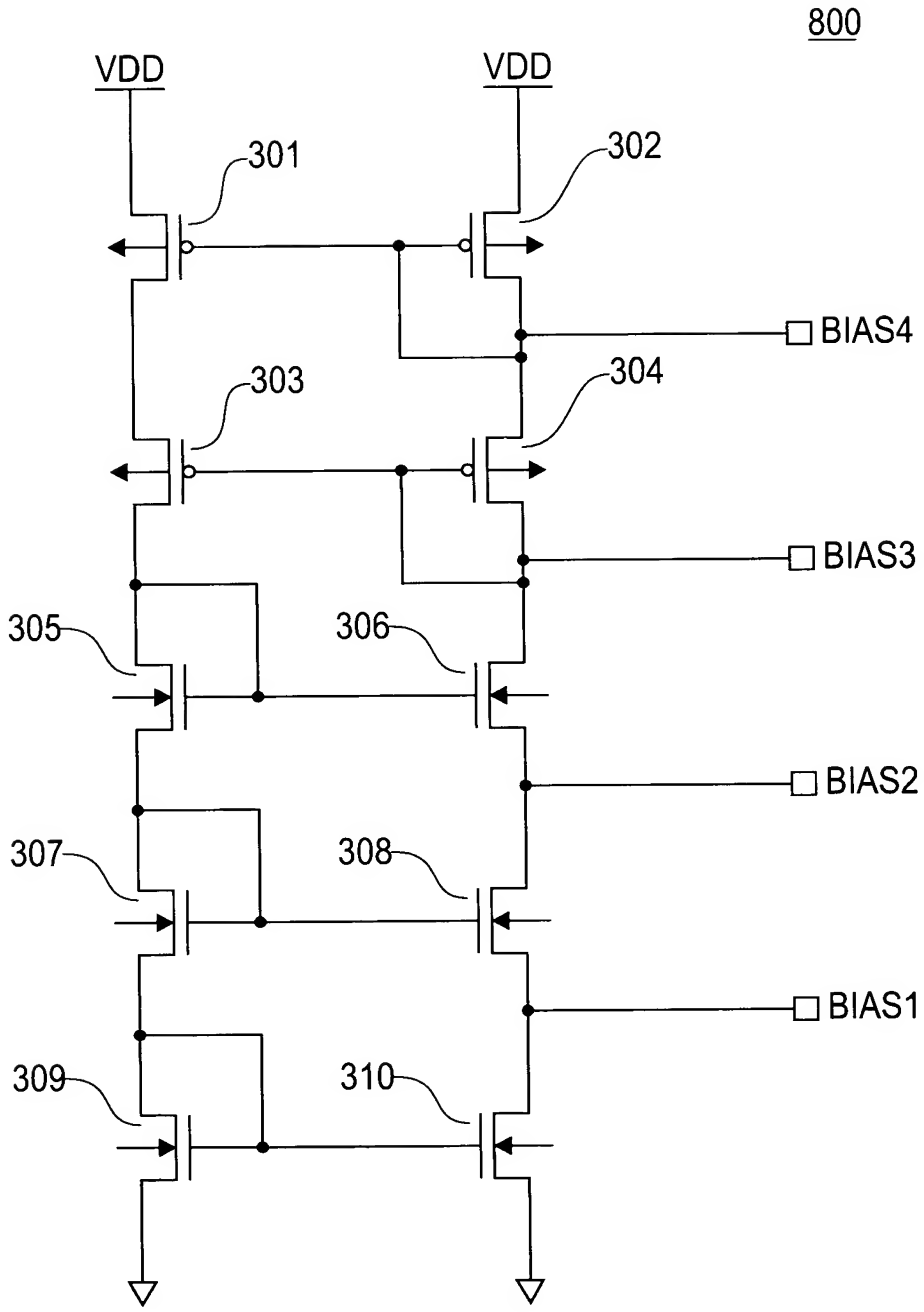
800
VDD
VDD
301
302
BIAS4
303
304
BIAS3
305
306
BIAS2
307
308
BIAS1
309
310

FIG.9

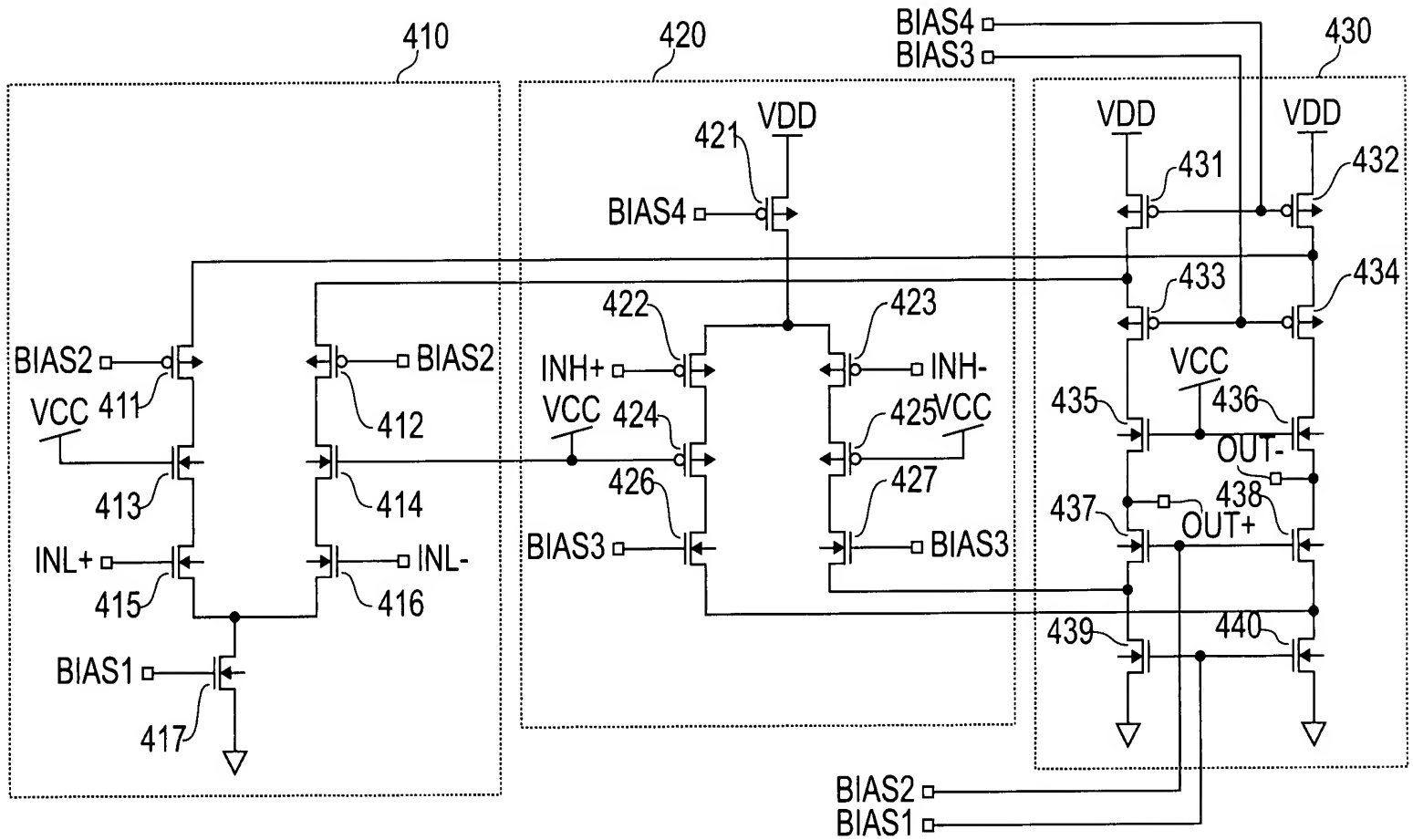
900
410
420
430
BIAS4
BIAS3
VDD
421
BIAS4
VDD
VDD
431
432
433
434
422
423
BIAS2
INH+
INH-
VCC
435
436
VCC 411
VCC 424
425 VCC
OUT-
412
426
427
438
437
OUT+
413
414
BIAS3
BIAS3
INL+
INL-
439
440
415
416
BIAS1
417
BIAS2
BIAS1

FIG. 10A

INPUT	OUTPUT
IN+ $>$ BIAS2	INH+ $\simeq$ IN+
IN+ $\leqq$ BIAS2	INH+ $\simeq$ BIAS2
IN+ $<$ BIAS3	INL+ $\simeq$ IN+
IN+ $\geqq$ BIAS3	INL+ $\simeq$ BIAS3

FIG. 10B

INPUT	OUTPUT
IN+ $>$ BIAS2	INH+ $\simeq$ IN+
IN+ $\leqq$ BIAS2	INH+ $\simeq$ BIAS2
IN+ $<$ BIAS3	INL+ $\simeq$ IN+
IN+ $\geqq$ BIAS3	INL+ $\simeq$ BIAS3